In the Claims:

1-6. (canceled)

7(currently amended). A packet processor comprising: ~~including a plurality of logic blocks, each logic block comprising:~~

a plurality of logical blocks, each of said plurality of logical blocks includes a sub-processor, said plurality of logical blocks pipelined in series with each other, each of said plurality of logical block operating independently of each other allowing concurrent processing of said plurality of sub-processors;

each of said plurality of logical blocks further including

an input receiving a first packet data associated with a first packet and a second packet data associated with a second packet;

a storage device storing the first packet data and the second packet data;

said a sub-processor coupled to the storage device, the sub-processor switching from processing the first packet data to processing the second packet data while awaiting a processing result for the first packet data.

8(original). The packet processor of claim 7, wherein the processing result is a conditional branch instruction result.

9(currently amended). A pipelined processor comprising a plurality of logic blocks connected in series, a first logic block for performing a first operation on a first processing instruction associated with a first packet and forwarding the first processing instruction to a second logic block for performing a second operation, the first logic block receiving a second processing instruction associated with a second packet if a potential stall is expected in processing the first processing instruction, the first logic block performing the first operation on

the second processing instruction concurrently with the second operation on the first processing instruction.

10(original). The pipelined processor of claim 9, characterized in that the first logic block receives a third processing instruction associated with the first packet if no potential stall is expected in processing the first processing instruction.

11(original). The pipelined processor of claim 9, wherein the potential stall is created by a conditional branch instruction.

12-19 (canceled).

20(currently amended). A method for processing packets in a pipelined processor having a plurality of logic blocks connected in series, the method comprising the steps of:

performing at the first logic block a first operation on a first processing instruction associated with a first packet;

forwarding the first processing instruction to a second logic block for performing a second operation; and

receiving at the first logic block a second processing instruction associated with a second packet if a potential stall is expected in processing the first processing instruction, the first logic block performing the first operation on the second processing instruction concurrently with the second operation on the first processing instruction.

21(original). The method of claim 20 further comprising the step of receiving at the first logic block a third processing instruction associated with the first packet if no potential stall is expected in processing the first processing instruction.

22(original). The method of claim 20, wherein the potential stall is created by a conditional branch instruction.